

**AMENDMENT AND RESPONSE**

Serial Number: 08/902,809

Filing Date: July 30, 1997

Title: SELECTIVE SPACER TECHNOLOGY TO PREVENT METAL OXIDE FORMATION DURING POLYCIDAL REOXIDATION

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**IN THE CLAIMS**

Please cancel claims 1-22 after adding new claims 23-43 as follows:

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23. [New] A semiconductor device comprising:  
an oxide active area;  
at least one feature over the oxide active area, the feature having a surface and being contiguous with the oxide active area at a boundary; and  
a spacer covering the surface of the feature and terminating at the boundary wherein the spacer is not in contact with the oxide active area.
24. [New] The semiconductor device of claim 23 wherein:  
the feature comprises an electrode including polysilicon, a refractory metal, and a dielectric, or undoped silicon;  
the spacer comprises silicon nitride or an amorphous silicon film; and  
the surface of the feature comprises sidewalls of the electrode.
25. [New] The semiconductor device of claim 23, further comprising a layer of oxide on the spacer and the oxide active area, the layer of oxide being formed by a polycide reoxidation and forming a smile at the boundary between the feature and the oxide active area.
26. [New] An electronic device comprising:  
a first layer of oxide;  
a feature over the first layer of oxide, the feature having a surface;  
a boundary between the first layer of oxide and the feature; and  
a spacer only on the surface of the feature.
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27. [New] The electronic device of claim 26 wherein the spacer is deposited on the surface of the feature extending to and terminating at the boundary.
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28. [New] The electronic device of claim 26 wherein:  
the first layer of oxide comprises a layer of gate oxide;  
the feature comprises an electrode including polysilicon, a refractory metal, and a dielectric, or undoped silicon;  
the spacer comprises silicon nitride or an amorphous silicon film; and  
the surface of the feature comprises sidewalls of the electrode.
29. [New] The electronic device of claim 26, further comprising a second layer of oxide on the spacer and the first layer of oxide, the second layer of oxide forming a smile at the boundary between the feature and the first layer of oxide.
30. [New] An electronic device comprising:  
a first layer of oxide;  
a feature over the first layer of oxide, the feature having a surface;  
a boundary between the first layer of oxide and the feature;  
a spacer only on the surface of the feature; and  
a second layer of oxide on the spacer and the first layer of oxide, the second layer of oxide forming a smile at the boundary between the feature and the first layer of oxide.
31. [New] The electronic device of claim 30 wherein:  
the first layer of oxide comprises a layer of gate oxide;  
the feature comprises an electrode including polysilicon, a refractory metal, and a dielectric, or undoped silicon;  
the spacer comprises silicon nitride or an amorphous silicon film and the spacer is deposited on the surface of the feature extending to and terminating at the boundary; and  
the surface of the feature comprises sidewalls of the electrode.

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32. [New] A semiconductor device comprising:  
a layer of a first material;  
a feature over the layer of the first material, the feature having a surface;  
a boundary between the layer of the first material and the feature; and  
a spacer only on the surface of the feature.
33. [New] The semiconductor device of claim 32 wherein the layer of the first material comprises a first layer of oxide.
34. [New] The semiconductor device of claim 33 wherein:  
the first layer of oxide comprises a layer of gate oxide;  
the feature comprises an electrode including polysilicon, a refractory metal, and a dielectric, or undoped silicon;  
the spacer comprises silicon nitride or an amorphous silicon film and the spacer is deposited on the surface of the feature extending to and terminating at the boundary; and  
the surface of the feature comprises sidewalls of the electrode.
35. [New] The semiconductor device of claim 33, further comprising a second layer of oxide on the spacer and the first layer of oxide, the second layer of oxide forming a smile at the boundary between the feature and the first layer of oxide.
36. [New] An electronic device comprising:  
a first layer of oxide;  
an electrode on the first layer of oxide, the electrode having sidewalls; and  
a spacer deposited only on the sidewalls of the electrode, the spacer extending to and terminating at a boundary between the first layer of oxide and the sidewalls of the electrode.

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37. [New] The electronic device of claim 36 wherein:  
the first layer of oxide comprises a layer of gate oxide;  
the electrode comprises polysilicon, a refractory metal, and a dielectric, or undoped silicon; and  
the spacer comprises silicon nitride or an amorphous silicon film.
38. [New] The electronic device of claim 36, further comprising a second layer of oxide on the spacer and the first layer of oxide, the second layer of oxide forming a smile at the boundary between the first layer of oxide and the sidewalls of the electrode.
39. [New] A semiconductor device, comprising:  
a first layer of oxide;  
a feature protruding from the first layer of oxide and having sidewalls, the feature including:  
a polysilicon portion;  
a portion of conductive material deposited on the polysilicon portion; and  
a spacer selectively deposited only on the sidewalls of the feature; and  
a second layer of oxide deposited on the semiconductor device, wherein the spacer is interposed between the second layer of oxide and the sidewalls of the feature.
40. [New] The semiconductor device of claim 39, wherein the spacer comprises silicon nitride or an amorphous silicon film and the portion of conductive material comprises tungsten silicide.

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12/ 41. [New] A semiconductor device, comprising:

a first layer of oxide;

a feature protruding from the first layer of oxide and having sidewalls, the feature comprising:

a layer of polysilicon;

one or more layers of conductive materials deposited on the layer of polysilicon,

wherein at least one of the layers comprises tungsten silicide; and

a silicon nitride spacer selectively deposited only on the sidewalls of the feature;

and

a second layer of oxide deposited on the semiconductor device, wherein the silicon nitride spacer is interposed between the second layer of oxide and the sidewalls of the feature.

42. [New] A gate electrode, comprising:

one or more layers of conductive materials etched to form a feature having sidewalls exposing the layers;

a selectively deposited spacer, wherein the spacer is deposited only on the sidewalls of the feature;

a layer of oxide disposed over the gate electrode.

43. [New] The gate electrode of claim 42, wherein the layers comprise tungsten silicide and the selectively deposited spacer comprises silicon nitride or an amorphous silicon film.

**REMARKS**

In response to the office action dated June 9, 1998, Applicant respectfully requests reconsideration of the application in view of the following remarks. Pending claims 1-22 have been canceled without prejudice and new claims 23-43 have been added to more particularly point out and distinctly claim the subject matter which the Applicant regards as the invention. No new matter has been added.

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